CLAIMS:

What is claimed is:

1. A method of measuring performance of a transceiver of a programmable logic device for jitter tolerance, comprising:

operating a receiver of the transceiver and receiving a data signal of a predefined serial data sequence;

recovering a clock signal from the data signal received;

detecting data bits from the data signal received using timing of the recovered clock signal;

comparing the data detected to reference data related to the predefined data sequence;

counting a number of error events resulting from the comparing over a duration encompassing a plurality of data bits of the predefined data sequence; and

quantifying performance of the receiver based on at least one of the count duration, the number of error events counted, and the predefined data sequence.

2. The method of claim 1, further comprising:

synchronizing the recovered clock relative to transitions of the data signal;

the detecting data to further comprise determining a framing event of a predetermined transfer protocol;

upon determining the framing event, reformatting respective plurality of serial data of the data detected into data words of a parallel bit format;

retrieving the reference data for the comparing from a data source preconfigured with data words of the same predefined data sequence; and

aligning the word sequences of the retrieved reference data to correlate with respective words to be detected from the data received;

the aligning based upon the framing event and synchronized with the recovered clock.

3. The method of claim 2, continuing the counting over a duration to encompass a statistically significant number of data bits of the predefined data sequence.

4. The method of claim 3, in which the framing event is of a non-return to zero protocol, and the aligning comprises:
detecting a comma from within a sequence of the detected data, and
responsive to detecting the comma, adjusting an index by which to retrieve a portion of the reference data related to the comma event of the same predefined data sequence.

5. The method of claim 4, further comprising configuring the predefined serial data sequence to comprise a stress sequence following the framing event, the stress sequence configured with consecutive, same-state data bits for a run-length greater than the maximum specified by the transfer protocol.

6. The method of claim 5, in which the non-return to zero protocol comprises an 8B/10B protocol and the stress sequence is configured for a run-length greater than 10 consecutive same-state bits.

7. The method of claim 5, further comprising:
determining an elapsed time relative to one of a predefined error probability or a jitter characteristic curve for

extending into the waterfall region of the characteristic curve; and

defining the run-length to the stress sequence based on the determined elapsed time.

8. The method of claim 5, in which the configuring the predefined serial sequence further comprises grouping a plurality of the framing events before the stress sequence.

9. The method of claim 8, in which the configuring the predefined serial sequence further comprises incorporating a conditioning preamble between the framing events and the stress sequence.

10. The method of claim 9, further comprising defining the conditioning preamble to last for a duration of at least one settling-time constant of a transfer function associated with the control-loop of the clock recovery circuit.

11. The method of claim 10, further comprising:

forming the conditioning preamble with multiple data state transitions per frame; and

using the conditioning preamble for at least a part of the synchronizing of the recovered clock.

12. The method of claim 3, wherein the comparing and the counting comprise:

comparing the reformatted data words relative to respective data words of the reference data to determine any differences therebetween; and

counting the number of comparisons yielding a difference determination.

13. The method of claim 3, wherein the comparing and the counting comprise:

comparing word-to-word the decoded data relative to that of the reference data; and

counting the number of bit errors therebetween.

14. The method of claim 2, further comprising:

sending to the receiver as a part of the predefined serial data sequence, a conditioning preamble followed by a stress sequence;

performing the synchronizing of the recovered clock during an interval of the data signal associated with the conditioning preamble; and

performing the comparing and the counting over an interval of the data signal associated with the stress sequence.

15. The method of claim 14, further comprising:

repeating a plurality of times the sending of the conditioning preamble followed by the stress sequence, the synchronizing of the recovered clock during the respective conditioning pattern repeats, and the comparing and the counting over the respective stress sequence repeats; and

combining the counts counted and basing the performance upon the combined count.

16. The method of claim 15, the plurality of repeats comprising N groups of M iterations, the method further comprising resetting at least a portion of the transceiver

circuitry between at least some of the groups of the N groups.

17. The method of claim 16, in which the resetting comprises:

reinitiating a phase lock loop acquisition for the clock recovery;

resetting buffers of the transceivers; and

re-framing data of the input data signal relative to framing events determined therefrom.

18. The method of claim 15, further comprising cycling the power of the transceiver between some of the iterations of the plurality of repeats.

19. The method of claim 1, in which the quantifying the performance comprises extrapolating a serial data transfer rate capability for the transceiver based upon the number of error events counted, the count duration and the predefined data sequence.

20. A method of testing the performance of a transceiver in a programmable logic device (PLD), comprising:

retrieving pre-determined test data from a first memory device;

multiplexing data words retrieved from the first memory to convert it from a word format into a serial format;

transmitting the serially formatted data by operating a transmitter of the transceiver;

receiving an input signal corresponding to the transmitted serially formatted data by operating a receiver of the transceiver;

detecting receive data from the input signal received;
de-multiplexing the detected receive data to convert it from a serial format to a word format;
retrieving reference data related to the predetermined test data from a second memory;
comparing the words de-multiplexed from the detected receive data to respective words of the reference data;
determining errors based upon the comparing;
counting any errors determined; and
rating a performance of the PLD based on the errors counted.

21. The method of claim 20, in which the receiving and the detecting of data from the input signal comprise:
sensing transitions of the received input signal;
generating a recovered clock;
controlling, with given control loop dynamics, the frequency of the recovered clock based upon the relative time placement of the transactions of the input signal with respect to those of the recovered clock; and
continuing the comparing and counting of the determined errors over a continuous duration substantially greater than the characteristic settling time constant associated with the control loop dynamics.

22. The method of claim 21, further comprising:
configuring the predetermined test data within the first memory to comprise a stress sequence of consecutive same-state data;
defining a run-length for the consecutive, same-state data to extend over a stress duration;

storing the same stress sequence for at least or part of the reference data in the second memory; and

performing the comparing and the counting over the stress duration of the stress sequence.

23. The method of claim 22, further comprising:

storing conditioning data in the first memory at a location thereof for retrieval as a preamble before the stress sequence;

when receiving the preamble portion of the input signal, using transitions of the conditioning pattern and synchronizing the recovered clock relative thereto; and

after the synchronizing of the recovered clock with the conditioning preamble and during an interval of time associated with receipt of the transmitted stress sequence, performing the retrieval of the reference data, the comparing, and the determining and the counting of errors.

24. The method of claim 23, further comprising repeating each of:

the retrieving, the multiplexing, and the transmitting to again transmit a preamble and stress sequence;

the receiving of an input signal corresponding to the transmitted serial data of the preamble and the stress sequence;

the retrieving of the reference data, the comparing and the determining and counting of errors; and

basing the performance rating upon the accumulated error counts.

25. The method of claim 24, further comprising:
performing the repeating a plurality of times; and
performing a power-down and power-up cycle of the transceiver with each of N groupings of M iterations of the plurality of repeats.

26. The method of claim 25, further comprising:
propagating the serial data from a transmitter of the transceiver to a receiver thereof along a transmission line configured with at least one of D.C. or A.C. coupling therebetween.

27. The method of claim 26, further comprising:
employing a framing event of a predetermined transfer protocol within the predetermined test data;
detecting the framing event within the sequential data of the input signed received;
correlating the data sequences of the reference data to be retrieved from the second memory so as to correspond with respective sequences of the predetermined test data expected from the de-multiplexed data; and
performing the correlating based upon the detection of the framing event.

28. The method of claim 20, in which the transmitting and the receiving are performed by respective transmitter and receiver circuits of the programmable logic device within part of internal self-testing of the programmable logic device.

29. A system for testing performance of a transceiver of an integrated circuit, comprising:

a first memory addressable to source predetermined test data, wherein the predetermined test data includes a stress sequence of a run length of same-state sequence of consecutive data bits;

a transmitter of the transceiver to receive data output by the first memory and to output it for propagation to a receiver of the integrated circuit;

the receiver to receive an input signal propagated from the transmitter;

a second memory addressable to source reference data related to the predetermined test data of the first memory;

a comparator to compare data received by the receiver to reference data retrieved from the second memory; and

a counter to count error events determined by the comparator.

30. The system of claim 29, further comprising:

a transmission channel to propagate the signal output from the transmitter to the receiver.

31. The system of claim 30, in which the transmission channel comprises an interconnect internal to the integrated circuit.

32. The system of claim 29, further comprising a processor to:

determine jitter performance of the transceiver based on the run-length of the same-state sequence configured for the test data, and the error count determined by the counter.

33. The system of claim 32, in which
the integrated circuit comprises a programmable logic device with selectably configurable resources;
the processor, the counter, the comparator, the first and second memory, the receiver and the transmitter embedded as a part of the programmable logic device;
the system further comprising a host programmer comprising configuration data to configure the configurable resources of the programmable logic device to:
route data from the first memory to a serializer of the transceiver and to by-pass a CRC encoder thereof;
enable a clock recovery circuit of the receiver to recover a clock signal from the data transitions of the received input signal; and
detect and de-serialize data of the input signal synchronous with the recovered clock.

34. The system of claim 33, the configuration data of the host programmer further to configure:
the first memory with a sequence of conditioning data as a preamble before the same-state consecutive sequence;
the clock recovery circuit to synchronize the recovered clock using the preamble portion of the receiver input signal; and
the run-length for a duration to substantially exceed a settling-time constant associated with the dynamic responsiveness of the clock recovery circuit.

35. The system of claim 34, in which the run-length is of a duration to exceed a maximum duration of a non-return-to-zero encoding protocol.

36. The system of claim 35, the processor further to cause a repeat for a plurality of times:

output from the transmitter of the preamble and the same-state, consecutive sequence;

synchronization of the recovered clock to respective preamble sequences; and

accrued counting by the counter of the respective error counts.

37. The system of claim 36, the processor further to cause resetting of at least portions of the transceiver between at least some of the plurality of repeats.

38. The system of claim 29, in which the integrated circuit comprises a programmable logic device with programmable resources selectably programmable to configure at least a portion of the first memory with the test data for transfer to the transmitter, the second memory with the reference data for transfer to the comparator, and the counter to count the errors determined by the comparator.

39. The system of claim 38, in which the programmable logic device further comprises configuration memory with configuration data by which to program the programmable resources for the system for testing performance.